

1/6

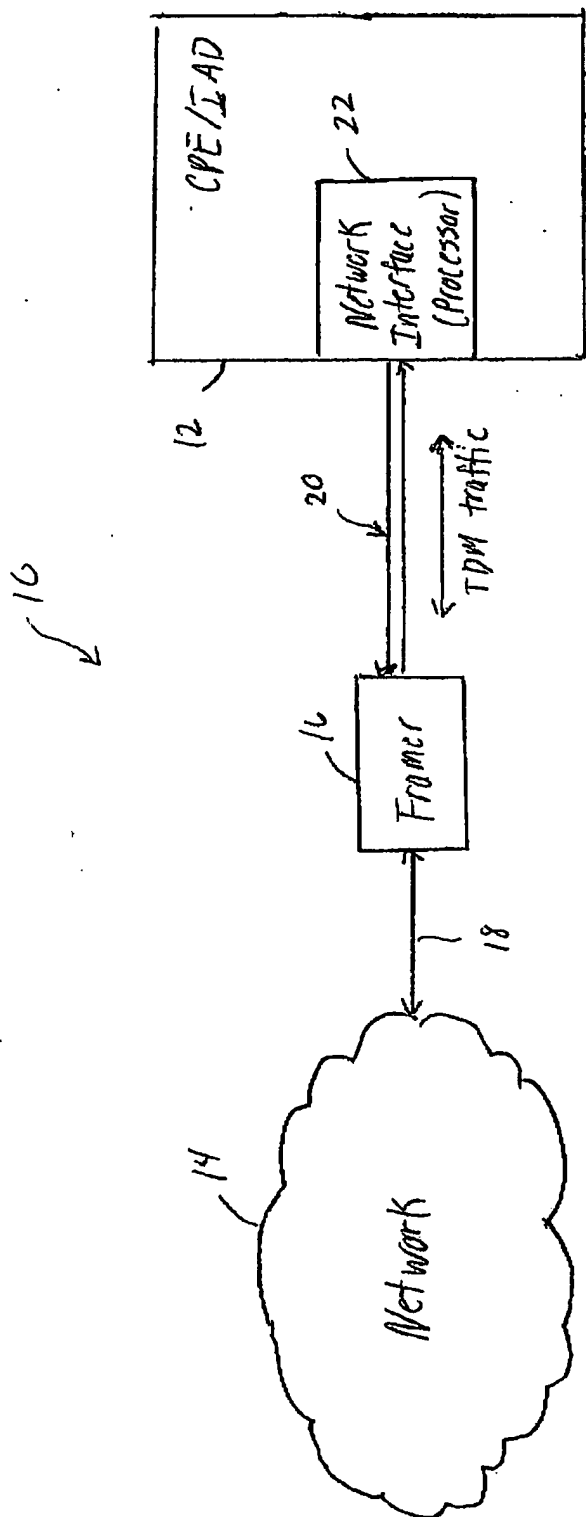


FIG. 1

CYCLE-EFFICIENT TDM TIMESLOT REMAPPING FOR NETWORK PROCESSING ENGINES

Daniel G. Borkowski et al.

INTEL-007PUS

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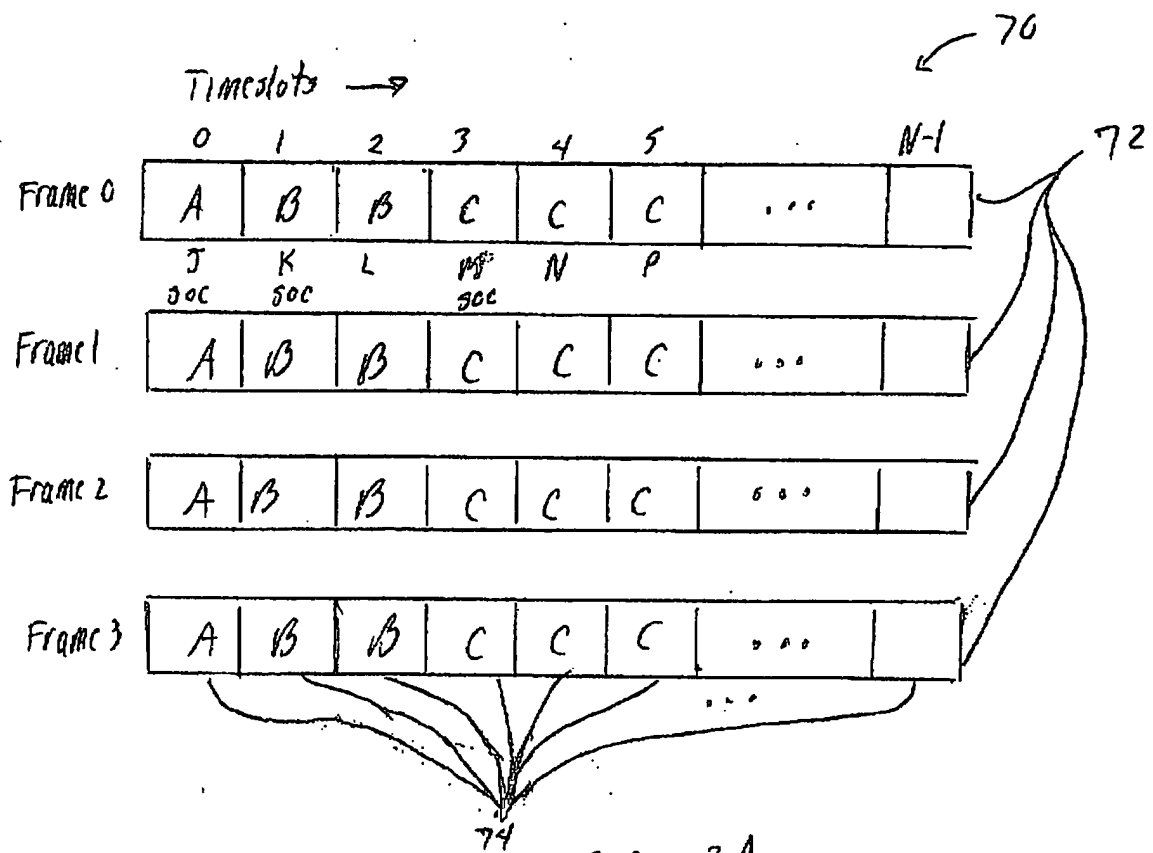


FIG. 3A

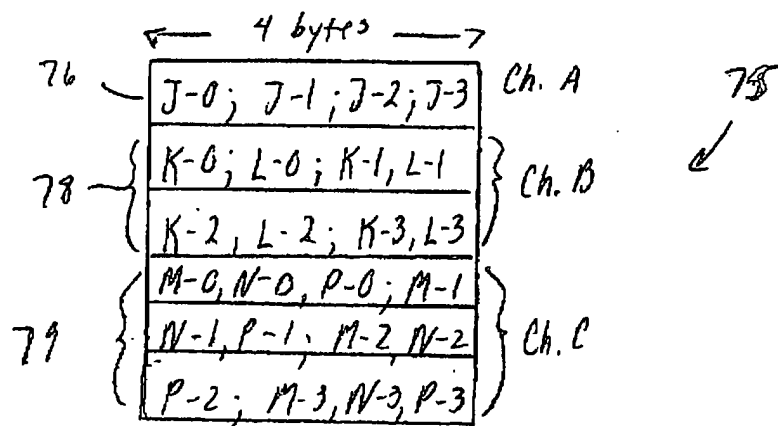


FIG. 3B

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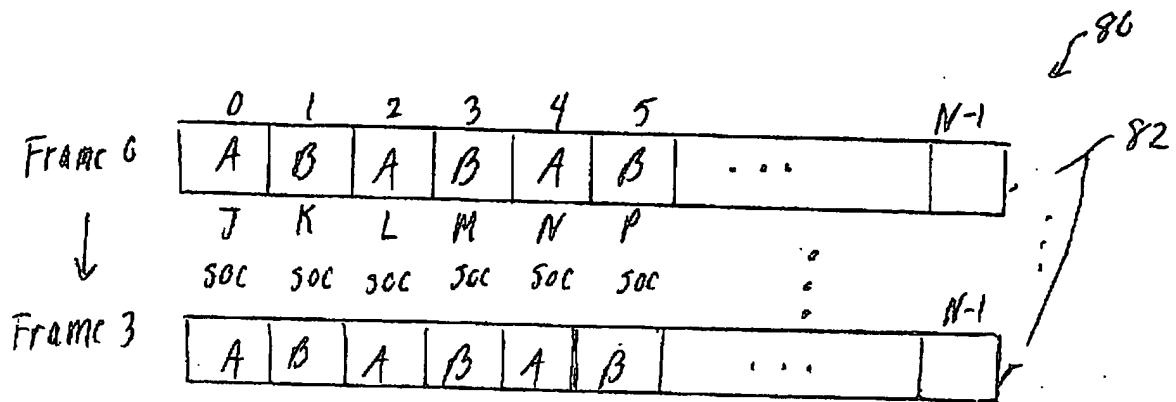


FIG. 4A

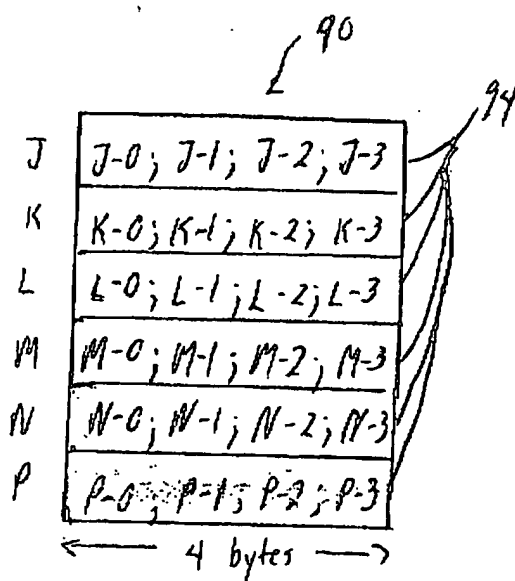


FIG. 4B

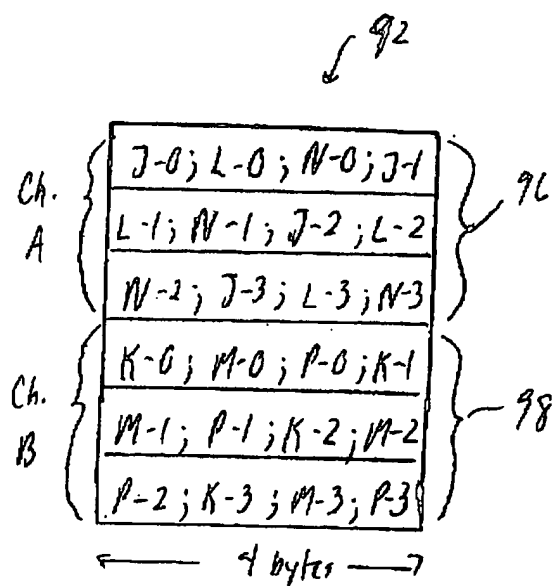


FIG. 4C

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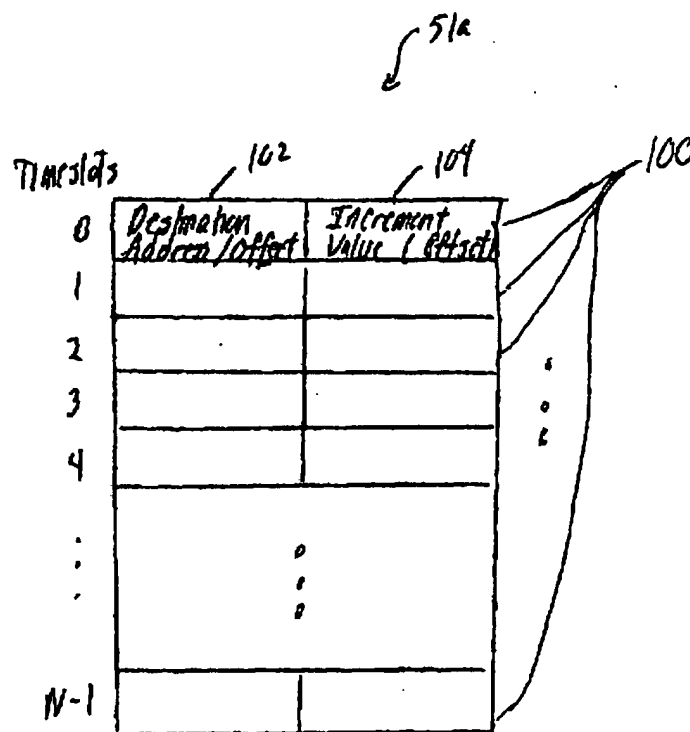


FIG. 5

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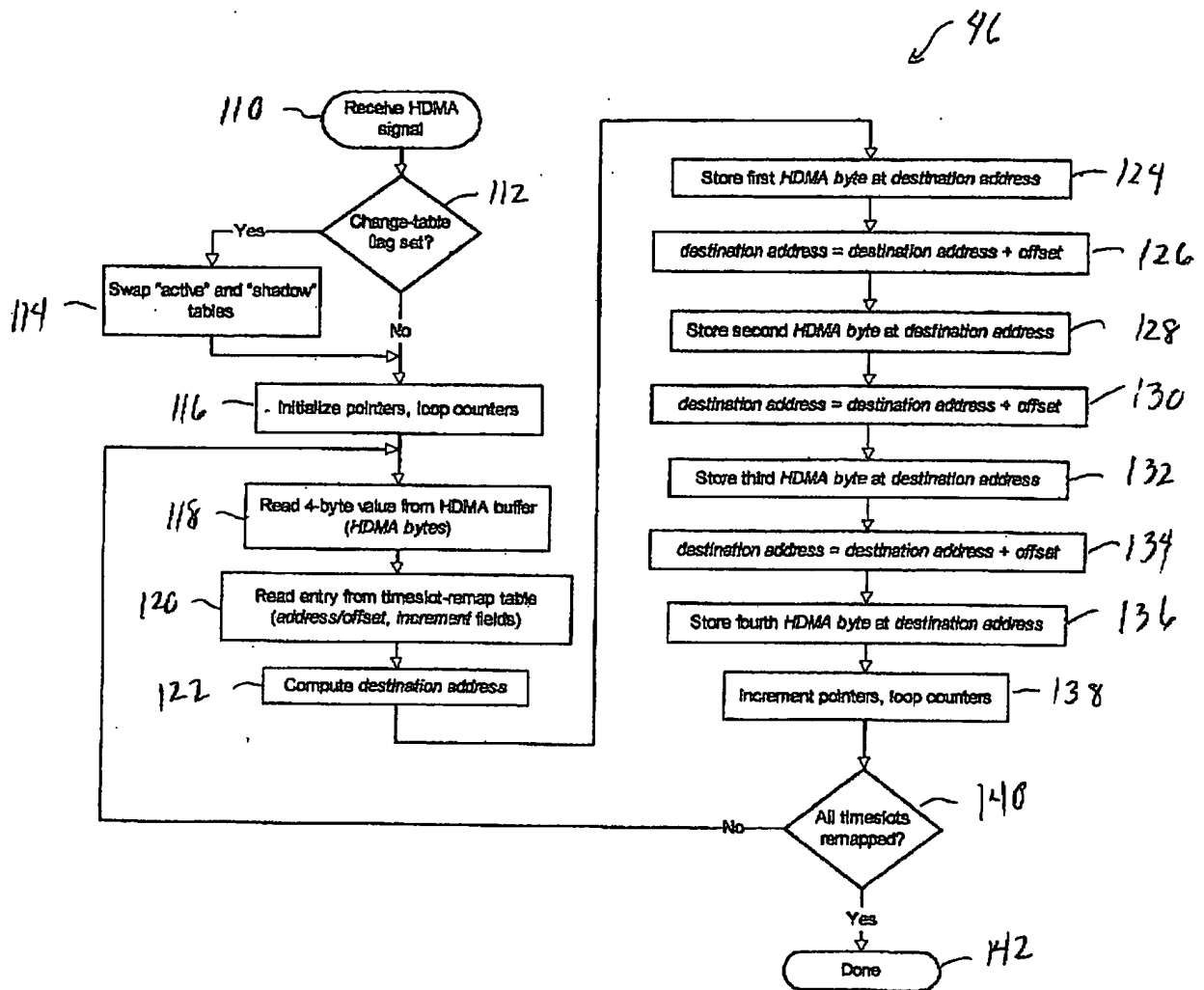


FIG. 6